**University of Queensland**

Optimization of a CPU Scheduler for Dark Silicon Parameters

A Thesis Project by Thomas Steel

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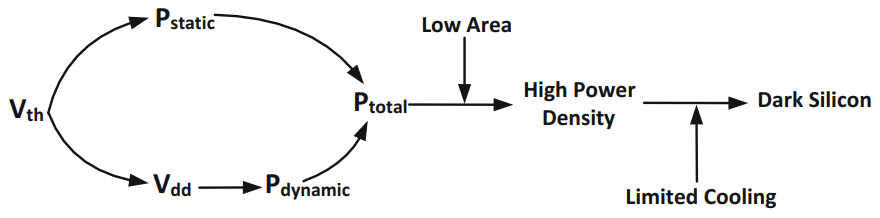
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# Topic Definition

Dark Silicon is the issue in modern computing where the assumptions of Moore’s Law and Dennard scaling break down. As the size of transistors reduces, we outpace our ability to cool the chips, leading to faster degradation when run for maximum performance. There is an additional energy-performance trade off, where chips cannot be powered at their maximum clock speed without exponential increases in energy requirements each generation. Alternatively, chips can use 40% less energy, with each generation but they will no longer be able to scale performance. This has led to an era constrained by Post-Dennard scaling, where doubling the number of transistors in a chip decreases creases the percentage of these transistors that are powered on at any given time.

The clearest description available that gathers the collective issues is found in the Dark Side of Silicon, by Rahmani et al., shown in Figure 1. While it is a simple model, it covers the collection of parameters that cause the dark silicon issue. The increasing power density of modern chips, without advancement in cooling technology, slowly leads to an increasing amount of silicon that cannot be powered.

Figure 1 - A simple diagram of dark silicon [8].

The term “dark silicon” refers to this silicon that is unpowered or being clocked significantly below its maximum frequency.

## Goals

This is a project to develop a CPU task scheduler on an FPGA that is optimised for dark silicon parameters. The goals of this thesis are:

* To develop an optimised softcore processor optimised through dark silicon methodologies
* To develop an optimised task scheduler for this processor optimised for resource allocation
* To produce a working kernel, with user and kernel modes, on this processor
* To fulfil the above goals by using the principles of dark silicon to advantage

## Relevance

The research space for dark silicon stretches from material scientists designing 3D silicon architectures or new transistor designs, to firmware and software engineers optimising resource allocation on the chip for these new parameters that must now be considered. There are also hardware approaches to of dark silicon, that focus on harnessing the principles to develop different styles of chips that steers into the metaphorical curve, using techniques such as heterogeneous cores, running cores at near threshold voltages and using computational sprinting to produce high throughput while conserving energy.

The scope of this project is being strictly limited to what can be implemented on an FPGA. This obviously precludes all approaches related to material science. Reducing the size of the cores to combat dim silicon will not be considered as it doesn’t harness the principles of dark silicon. Dim silicon methodologies such as computational sprinting and underclocking are within the scope, but dynamic voltage scaling is not, as it requires additional modules that add a significant amount of complexity to the design and testing. Heterogeneous multicores are in scope as they represent an important way to scale up computational efficiency. CPU scheduler design methodologies and resource allocation techniques are in scope as they will be required to capitalise on the optimisation at the hardware level. Finally, an approach to computing that weaves between several of the above methods know as memory driven computing is within the scope, as it represents an important possible future in the era of dark silicon.

# Literature Review

## Obituary for Moore’s Law and Dennard Scaling

In his seminal document on the subject, Gordon E. Moore predicted an exponential increase in the number of transistors in an integrated circuit [1]. As shown in Figure 1, this exponential law has become less relevant in the past 20 years, in a way that is largely explained by factors that represent the downfall of Dennard scaling [2].

Figure 2 – Historical data for the last 20 years of chip development [2].

Blue circles represent SRAM density.  
Green Triangles represent minimum wire-to-wire spacing.  
Red Squares show minimum spacing between transistors.

The companion of Moore’s Law is Dennard Scaling. In 1974, Robert H. Dennard released a paper describing the scaling of MOSFET devices [3], a scaling which held alongside Moore’s Law until decreasing transistor size resulted in an increase in the significance of physical constraints on the scaling of circuits. In a 33 year retrospective in 2007, assumptions that underlay Dennards scaling failed. For example, Dennard assumed that there would be a continual increase in channel doping concentration that would allow continuously shorter channel lengths. However, as the doping concentration increases, impurity scattering causes degradation of carrier mobility and performance [4].

## The mimimum energy for computing

In the last century, it was proven by Charles H Bennet and Ralph Landauer that for any irreversible computation, there is a minimum energy required required per switching equal to kBTln2, approximately 10-21J at room temperature. This is called the Shannon-von Nuemann-Landauer limit, and it describes the physical limits of switching elements, such as a CMOS transistor. This is relevant because it helps to explain the issue of dark silicon: that the transistors are not, in modern microprocessors, the primary source of energy consumption. Energy consumption in electronics is primarily caused by electrical capacitances. In modern microprocessors in the 22-65nm node range, ~20-30% of the total energy consumed is attributed to transistors, a percentage that is expected to reduce as transistors become smaller. This is caused by an inverse relationship between leakage currents and transistors size. The other significant losses are due to interconnects (e.g. wires) [5]. The wire interconnects can be modelled as capacitive lumps in the case of short wirse, lossy RC transmission lines the case of medium length wires, and long global wires need to be modelled as lossy RLC transmission lines. As scaling increases, these wire interconnects become the dominant limitting factor in terms of clocking frequency, delay, power and area [5, 6].

## The Four Horsemen of Dark Silicon

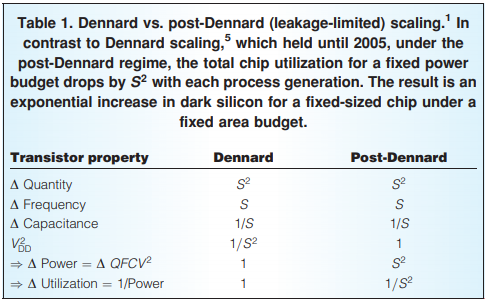
As Dennardian scaling breaks down, the period of Post-Dennardian scaling arises, shown in Table 1. There is an exponential reduction in the percentage of silicon in a chip that can switch at full frequency that decreases with every generation. An important result of this is that multicore scaling becomes prohibitive as it produces large amounts of dark silicon. Taylor, in an early survey of the dark silicon problem, defined 4 “horsemen” as solutions for the challenge of dark silicon. Ordered from most to least relevant, these are

Table 1 - Ratio’s for Dennard and Post-Dennard scaling [9].

* The Specialised Horseman defined by a new age of Heterogenous core design
* The Dim Horseman focusses on spreading the same power budget over more transistors
* And the Shrinking Horseman, which removes dark silicon by reducing the size of the die
* The Deus Ex Machina Horseman where technological advancement nullifies the issue.

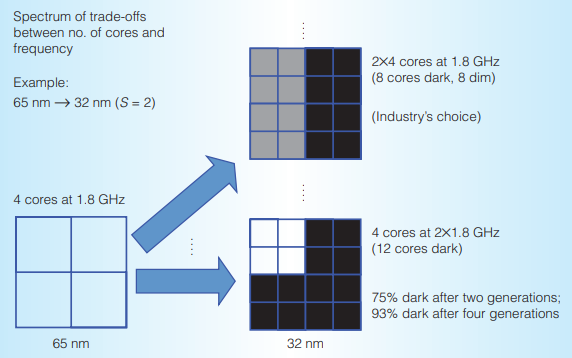
The Specialised Horseman relies on the principle that ASIC circuitry is usually 100 to 1000x faster than general processing units, and that general processing units typically use 157 to 707x the energy of an ASIC circuit for a similar task [7]. Heterogeneous cores and computational accelerator are both possible answers to the inefficiencies of modern CPU’s [8, 9].

Figure 3 - A graphical example of the dark silicon [9].

The Dim Horseman, focussed on dim silicon methodology, relies on underpowering or underclocking portions of the chip. Near Threshold Voltage processors and Dynamic Voltage and Frequency Scaling are both successful methods for this. Near Threshold Voltages, the voltage across the transistors is reduced to a point that is optimal for energy delay. This point is the lowest voltage that can be used without requiring a steep drop in frequency. Although intriguing, it requires additional hardware that increases the complexity of this project [10]. Whilst Dynamic Voltage Scaling is precluded for the same reason, Dynamic Frequency Scaling can be implemented with appropriate use of prescalers and will be pursued as a possible source of optimisation.

Another popular method is computational sprinting, where the chip spends most of the time in a low-performance state but moved into a high-performance state for brief periods, or a second core is activated for a brief period. This brief period is a sprint and can be implemented to increase the energy efficiency as the resource of the extra CPU can be allocated as needed, and short operations can be sprinted through allowing the chip to go idle afterwards. This helps to manage the energy and thermal issues of dark silicon [11].

The Shrinking Horseman refers to the design approach of simply designing smaller processors using less chip space to not go above the power budget on the chip.

The Deus Ex Machina horseman represent new technologies, such as the QFET, the GAA transistor model, or perhaps the transistors that can be achieved through using diamond as the conducting material. Future projects on optimising a CPU scheduler for their parameters would be compelling. It stands to reason, these things being the focus of data science, that this is entirely out of scope [9].

## Memory Driven Computing

Memory driven computing occurs as a solution to the intense power usage of interconnects and memory blocks. In standard computing, memory is stored at varying distances and sizes with the focus being on the computing unit. In memory driven computing, the memory is the focus and the processing is on the periphery. This is an intuitive answer to the problems presented by an increased prominence of wire and memory costs. As computing move into a period where there are diminishing returns on computational performance due to externalities, switching the design focus to these externalities could prove to be a bountiful approach [12].

## The Dark Side of Silicon

In the Dark side of Silicon, Rahmani et al. describe a suite of methodologies for managing dark silicon. The heterogeneous methodology gives more direction than that of Taylor, but the section of interest is the management in the OS layer. Variation-Aware Core Selection and Scheduling is a methodology for efficient resource allocation within the power budget constraints of dark silicon [8, 13].

The Dark Side of Silicon suggests the SiLago methodology for implementing and exploiting heterogeneity. In a problem analysis of the industry, 4 issues became apparent:

Figure 4 - Design methodologies for dark silicon

* Most design focussed on the cores, ignoring the memory and interconnects
* Software abstraction relies on naïve resource allocation, resulting in inefficiencies at runtime
* The lack of dynamic runtime customization means that non-deterministic concurrency and communication patterns result in inefficiency power usage and parallelism
* Customisation has a large engineering cost that make it prohibitive.

The SiLago platform attempts to solve these problems by implementing a Distributed Memory Architecture. This is a form of memory driven computing and has been shown to have significant reductions in power and energy expenditure if done properly [14]. Similar methodologies have found that by arbitrarily spacing memory throughout a chip, the power cost of on-chip interconnects can be severely reduced [15].

## CPU Scheduling

CPU scheduling is concerned with a number of things

* CPU utilisation, keeping the CPU running as often as possible
* Data throughput, a measure of CPU utilisation
* Turnaround time, the period it takes for a process to be completed
* Waiting time, how long the process spends waiting to use the CPU,
* And response time, the time between when a process is put onto the queue and when the first response is produced

Algorithms for scheduling tend to focus on the priority of tasks first, and the allocation of resources second. An example of this is a Priority Scheduler, which weighs the priority of incoming tasks and parcels out operating time based on precedence of priority. A more complex and relevant method however is a Multilevel Feedback Queue, which prevents any single process from taking up too much time. [16]

## Why Heat is not a Metric

Given the nature of dark silicon, it seems intuitive to use heat as a metric for progress. This approach is hobbled by the stumbling black that is the difference between the physical model of a microprocessor and an FPGA. While it is possible to gain considerable improvements to efficiency with thermal aware design designing, this increases the complexity and requires optimisation and tuning that is device specific. Gains from thermal aware design would not necessarily translate between devices, and so more translatable measures and improvements will be the focus of this project [17, 18].

# The Gap in the Knowledge

A pair of theses that run in parallel this this project are Scheduling Dark Silicon by Andrew Tomlinson and Energy-efficient Scheduling for Heterogeneous Servers in the Dark Silicon Era by Sankalp Jain.

Scheduling dark silicon focusses on computational modelling heterogeneous core operation and optimising the threading for this system [19].

Energy-efficiency Scheduling for Heterogeneous Servers similarly has a tighter focus on optimising a specific core fore a specific use case. In his thesis, Jain optimised a multi-core system to produce better performance and energy efficiency through better scheduling policies [20].

This project has a focus on practical application and producing comparable data through experimental design methodology. It also has a greater focus on the hardware layer than these other projects, and there is the added complexity that both the hardware and OS layers in this project have dependencies on each other. This project will therefore tend to have a heavier focus on fitting the hardware to suit the OS layer, as the OS layer has already been well researched and developed.

# System Overview

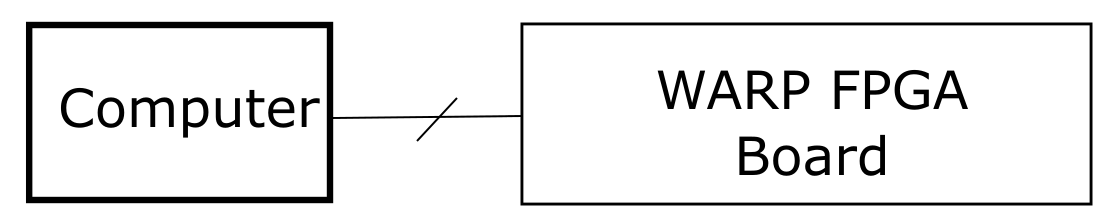


Figure 5 – Hardware diagram of project configuration

The hardware for this project will consist a computer and an FPGA, with a RISC-V core implemented on it. The internal design of the core will vary as the design develops across the project.

# System Integration

No sensors are required. Data will largely be drawn from Xilinx and CAD.

# Algorithm Schemes

Testing for the scheduler will include a round robin system, a priority queue system and a hybridised system, to give a range for the data.

The Variation-Aware Core Selection and Scheduling will also be an important methodology for reducing the amount of naïve scheduling caused by abstraction away from the hardware layer [13].

# Performance Indicators

A basic control dataset will be produces using the RISC-V core with a basic Linux system run on the softcore. This will test for:

* Data Throughput
* Power and energy requirements
* Area of chip used
* Clocking Frequency
* Data integrity
* Cycles per operation
* Quality of Resource allocation

These metrics will be used as a baseline to contrast the CPU core against as it is developed.

# List of Equipment Required

For this thesis project, a computer that can synthesis FPGA bitstreams is required, as it an FPGA board.

* FPGA – Rice University WARP FPGA Board [21]
* Oscilloscope
* Computer

# Technology Readiness Level

TRL 1 – Task scheduler optimised, metrics show improvement over naïve resource allocation.

TRL 2 – Task scheduler showing clear links between target optimizations and metrics and can process basic datasets.

TRL 3 – Task scheduler can be used to process moderately complex, sanitized datasets.

TRL 4 – Task scheduler running Linux with evidence of optimisation

TRL 5 – Task scheduler, under controlled circumstance and settings, can be used as a basic general-purpose computing system, shown to work on range robust datasets.

TRL 6 – Task scheduler performing optimal resource allocation for a variety of datasets. Can be used as general use computing system.

# Project Plan

The project milestones will mostly be marked in hardware, with hardware and firmware development being done in tandem. The goal is to develop several separate approaches (computational sprinting, heterogeneous cores and memory driven computing focusses) alone and then to test combined syntheses of these approaches, with the most promising design being using to implemented and tested on complex datasets.

# Project Schedule and Timeline

30/08/19 – All equipment confirmed to be working, RISC-V softcore implemented on FPGA, Linux system running on pre-optimised RISC-V core.

13/09/19 – Control testing of metrics, sensitivity testing of metrics, control data collected from Linux.

11/09/19 – Seminar Prepared. Begin optimisation for computational sprinting.

27/09/19 – Testing on basic datasets for computational sprinting.

08/10/19 – Begin optimisation for memory driven computing.

25/10/19 – Testing on basic datasets for memory driven computing.

08/11/19 – Testing basic datasets for memory driven computing with computational sprinting.

22/11/19 – Begin testing Linux on optimised core for benchmark.

13/12/19 – Begin work on heterogeneous cores.

24/01/20 – Test basic datasets with heterogeneous cores. Should have 30 pages of thesis drafted.

07/02/20 – Test basic datasets with heterogeneous cores and computational sprinting.

21/02/20 – Test basic datasets on heterogeneous cores with memory driven computing.

06/03/20 – Test all 3 methodologies together, finalise plans for final design.

20/03/20 – Implement core, begin testing on complex datasets. First draft of thesis complete.

10/04/20 – Implement project as general computer with TRL of 6.

17/04/20 – Second draft of thesis complete.

15/05/20 – Poster and demonstration prepared.

08/06/20 – Thesis completed and submitted.

## Progress

As of the deadline of this thesis proposal, the scope and intention of the project have been identified, with methodologies outside of the scope of this project being rejected. A clear plan has been formulated, an FPGA has been chosen and a softcore processor has been elected.

# Conclusion

Dark silicon is a roadblock on the path to future performance increases, forcing us to pick and choose which mutually exclusive parameters of a chip we wish to optimise to the detriment of the remaining parameters. In this thesis, by increasing the complexity of design and moving away from naïve resource allocation, a point of balance will be explored that allows for high throughput whilst maintaining some of the energy efficient gains that new generations of transistors will produce.

By producing and comparing a set of optimised softcore processors with a firmware layer optimised for appropriate resource allocation between tasks, this project will produce a core optimised for dark silicon parameters.

## OHS and Ethics

This project has no ethical dilemma’s present in it.

### Risk Assessment

This project involves a small amount of hardware in the form of an FPGA board with a power source, and a module to attach external memory. This risk assessment is required due to the use of the Medium Risk Axon 201 Lab.

A list of rules for the laboratory can be found at <http://www.itee.uq.edu.au/laboratory-rules>.

These rules will be followed to the letter.

A more specific set of risks that will apply should additional handmade modules be required are as follows.

Medical attention refers to anything from burn cream and a band aid to being taken to the ER. This must be gauged at the time. A first-degree burn requires water, burn cream and a bandage. Cutting a vein requires immediate attention at a hospital. Adequate judgement must be employed in the moment. If there is uncertainty as to the medical requirements

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Hazard | Risk Rating | Risk Control | Hazard Event | Event Procedures |
| Oscilloscope | Low | Always have care and pay attention when using oscilloscope. | Electrocution | Ensure power has been switched off. Call an ambulance and secure the area. |
| Function Generator | Low | Always have care and pay attention when using function generator. | Electrocution | Ensure power has been switched off. Call an ambulance and secure the area. |
| Wall Plug Power Source | Low | Always have care and pay attention when using wall plug. | Electrocution | Ensure power has been switched off. Call an ambulance and secure the area. |
| Logic Analyser | Low | Always take care and pay attention when using the logic analyser. | Electrocution or electrical burn | Unplug logic analyser, |
| Soldering Iron | Medium | Take care and pay attention when using soldering equipment. Always wear PPE. | Injury or burn caused by soldering iron | Immediately turn off and replace soldering iron in holder. Apply cold water or ice to injury and seek medical attention. |
| Reflow Gun | Medium | Take care and pay attention when using reflow equipment.  Always wear PPE. | Burn caused by reflow gun | Immediately turn off and replace reflow gun in holder. Apply cold water or ice to injury and seek medical attention. |
| Hand Tools | Medium | Take care and pay attention when using any hand tools. | Sharps injury caused by hand tools. | Immediately seek medical attention for wound, report tool to appropriate authorities for sterilisation. |
| Low Voltage Environment | Medium | Pay careful attention to surrounding environment, keeping appropriate distance from any project that is an unknown variable. | Electrocution | Ensure power has been switched off. Call an ambulance and secure the area. |

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